AMENDMENTS TO THE CLAIMS

1. (Previously presented) A method of reducing circuit timing delays, comprising:

selecting a first node;

sorting fanins of the first node according to slack values associated with the corresponding fanins, wherein at least a portion of the slack values differ in value; and

reducing delays associated with fanins having relatively larger negative slack values before reducing delays associated with fanins having relatively smaller negative slack values.

2. (Original) The method defined in Claim 1, wherein reducing delays is performed recursively.

3. (Original) The method defined in Claim 2, wherein recursively reducing delays is performed until the delays cannot be further reduced or timing constraints are violated.

4. (Original) The method defined in Claim 1, wherein selecting the first node comprises:

performing a timing analysis on a circuit;

determining a delay target based at least in part on the timing analysis;

determining a slack value for each critical node of the circuit based on the delay target; and

sorting the critical nodes based on the corresponding slack values.

5. (Original) The method defined in Claim 4, wherein selecting the first node further comprises selecting a critical node having the largest negative slack.

6. (Original) A method of reducing circuit timing delays, comprising:

selecting a first node;

identifying critical fanins of the first node; and

recursively reducing delays associated with at least a portion of the critical fanins of the first node.

7. (Previously presented) The method defined in Claim 6, wherein recursively reducing delays is performed on critical fanins having relatively larger negative slack values before reducing delays associated with fanins having relatively smaller negative slack values.

8. (Original) The method defined in Claim 6, additionally comprising performing a local transformation on the first node if the reducing delays for at least one of the critical fanins is not successful.

9. (Previously presented) A method of performing circuit delay reduction, comprising:

performing a timing analysis on a circuit;

determining a delay target based at least in part on the timing analysis;

selecting a first output having a negative slack based at least in part on the delay target and the amount of first output negative slack relative to the slack of other outputs; and

performing local transformations on transitive fanins of the first output to improve the negative slack.

10. (Original) The method defined in Claim 9, wherein the first output is a critical output.

11. (Previously presented) A method of reducing timing delays for a circuit having primary input (PI) nodes, at least one primary output (PO) node, and a set of circuit nodes between the PI nodes and the PO node(s), the method comprising:

a) identifying a first critical path between a first PI node and a first PO node, wherein the first critical path is selected based on ordering the PO nodes by corresponding slack values;

b) beginning at the first PO node, attempting to reduce a delay associated with a first circuit node;

c) determining if the delay reduction meets a first predetermined criteria;

d) identifying a following circuit node in the critical path if the predetermined criteria is not met;

e) attempting to reduce a delay associated with the following circuit node;

f) repeating c), d) and e) until the delay cannot be reduced or a set of constraints are violated;

g) identifying a second critical path between a second PI node and a second PO node, wherein the second critical path is selected based on the ordered PO nodes;

h) determining an amount of delay reduction still needed for the second critical path after applying the results of the delay reduction for the first critical path; and

i) beginning at the second PO node, attempting to reduce a delay associated with a second circuit node.

12. (Canceled).

13. (Original) The method defined in Claim 11, wherein a critical path is a path that needs to be reduced in delay so as to meet a target timing constraint.

14. (Original) The method defined in Claim 11, additionally comprising establishing the criteria.

15. (Original) The method defined in Claim 11, wherein the method is performed at a logic optimization phase of a circuit design process.

16. (Original) The method defined in Claim 11, wherein the method is performed at a mapping phase of a circuit design process.

17. (Original) The method defined in Claim 11, wherein the method is performed at a layout phase of a circuit design process.

18. (Previously presented) The method defined in Claim 11, wherein the first PI node and the second PI node are the same.

19. (Previously presented) The method defined in Claim 11, wherein the first PO node and the second PO node are the same.

20. (Previously presented) The method defined in Claim 11, wherein a portion of the first critical path overlays a portion of the second critical path.

21. (Currently amended) A method of dynamically reducing delays on a critical path of a circuit topology, the method comprising:

identifying a critical path of the circuit topology;

selecting a delay target for a primary output associated with the critical path;

dynamically reducing a first critical path delay at a first node in closer proximity to a primary input associated with the critical path than to a node in closer proximity to the primary output;

storing the reduced delay; and

recursively dynamically reducing a second critical path delay beginning at a second node located between the first node and the primary output based at least in part on the stored reduced delay.

22. (Previously presented) The method defined in Claim 21, wherein the circuit topology is associated with a standard cell design process.

23. (Previously presented) The method defined in Claim 21, wherein the circuit topology is associated with a gate array design process.

24. (Previously presented) The method defined in Claim 21, wherein the circuit topology is associated with a programmable logic design process.

25. (Currently amended) A layout-driven logic synthesis design flow, comprising:

selecting a desired circuit delay associated with a first output of a circuit path, wherein other outputs are associated with different initial circuit delays;

calculating an initial circuit delay associated with the first output; and

iteratively reducing the initial circuit delay to achieve the desired circuit delay using a timing optimization process, wherein in an iteration, mapping and clustering are used to measure the outcome of the timing optimization procedure, and wherein the timing optimization process uses such measurements to achieve the desired delay, and wherein the result of an iteration of delay reduction is used by a next iteration of delay reduction to determine an amount of delay to reduce.

26. (Previously presented) The method defined in Claim 25, wherein the design flow is associated with a standard cell design process.

27. (Previously presented) The method defined in Claim 25, wherein the design flow is associated with a gate array design process.

28. (Previously presented) The method defined in Claim 25, wherein the design flow is associated with a programmable logic design process.

29-31. (Canceled).

32. (Currently amended) The method defined in Claim 1, additionally comprising performing a local transformation on the first node if the reducing delays for at least one of a set of fanins with negative slack values of the first node is not successful.

33. (Previously presented) The method defined in Claim 1, wherein reducing delays associated with the fanins of the first node is performed before any local transformation of the first node.

34. (Previously presented) The method defined in Claim 1, wherein sorting fanins of the first node includes sorting fanins of the first node in order according to slack values associated with the corresponding fanins.

35. (Previously presented) The method defined in Claim 1, wherein reducing delays associated with the fanins of the first node comprises:

a) computing a delay target for each of the fanins;

b) determining if an arrival time for a one of the fanins is greater than the delay target for the one fanin;

c) performing a delay reduction on the one fanin recursively if the arrival time for the one fanin is greater than the delay target for the one fanin; and

d) repeating b) and c) for a next fanin of the first node.

36. (Previously presented) The method defined in Claim 35, wherein reducing delays associated with the fanins of the first node further comprises stopping after c) if the delay reduction of one of the fanins is not successful.

37. (Previously presented) The method defined in Claim 35, wherein the delay target for a particular fanin is based on a delay target of the first node, a pin-to-pin delay of the particular fanin, and an interconnect delay from the particular fanin.